BRIEF FOR APPELLEE

DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

United States Court of Appeals
for the Federal Circuit

Appeal No. 03-1121
(Serial no. 08/568,904)

IN RE LAVAUGHN F. WATTS, JR.

Appeal from the United States Patent and Trademark Office,
Board of Patent Appeals and Interferences.

JOHN M. WHEALAN
Solicitor

THOMAS W. KRAUSE
JOSEPH G. PICCOLO
Associate Solicitors

P.O. Box 15667
Arlington, Virginia 22215
(703) 305-9035

Attorneys for the Director of the United States Patent and Trademark Office

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Representative Claims:

5. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a monitor for monitoring temperature within said apparatus; and

a clock manager adapted to receive a control signal from said monitor, said clock manager selectively stopping clock signals from being sent to said central processing unit (CPU) when said monitored temperature rises to a level at and above a selected reference temperature level and said CPU is not processing critical I/O.

A328.

17. A computer, comprising:

means for sampling a temperature level associated with the operation of a central processing unit within said computer;

means for predicting temperature levels associated with the operation of a central processing unit within said computer; and

means for using said prediction for automatic control of temperature within said computer, said temperature control remaining transparent to a user of said computer.

A329.

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RULE 47.5 STATEMENT OF RELATED CASES

(a) No other appeal from the Board of Patent Appeals and Interferences in connection with the patent application on appeal has previously been before this or any other court.

(b) Co-pending Appeal 03-1122 (Fed. Cir.), also In re Watts, is related to subject appeal 03-1121 because the two appeals share the following commonalities:

1. inventor LaVaughn F. Watts, Jr.;
2. assignee Texas Instruments Inc.;
3. immediate parent patent application (08/023,831 (A121[1]));
4. similar application specification and title;
5. application filing date in same month (December 1995);
6. technology of placing a CPU in sleep mode in view of thermal management;
7. USPTO examiner, art unit, subclass, and class;
8. applied prior art reference issued to Kikinis;
9. counsel of record for appellant;
10. counsel of record for appellee;

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[1] The Appendix is referred to as "A___".

RULE 47.5 STATEMENT OF RELATED CASES (cont.)

11. USPTO final decisions issued in same month (August 2002);

12. Appellant notices of appeal filed in same month (October 2002); and

13. Court briefing is expected to conclude around the same time.

Accordingly, for the above reasons, *and* in the interest of judicial economy, the Director believes that the Court may wish to consider assigning 03-1121 and 03-1122 to the same judicial panel.

BRIEF FOR APPELLEE
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

United States Court of Appeals
for the Federal Circuit

Appeal No. 03-1121
(Serial no. 08/568,904)

IN RE LAVAUGHN F. WATTS, JR.

Appeal from the United States Patent and Trademark Office,
Board of Patent Appeals and Interferences.

STATEMENT OF THE ISSUE

Representative claim 5 claims a central processing unit ("CPU") with a "clock manager" that "selectively stop[s]" clock signals from being sent to the CPU if (i) the CPU temperature rises above a reference level so long as (ii) the CPU is not processing critical I/O (input/output). The Board affirmed the obviousness rejection of claim 5 given that (1) Hollowell teaches a CPU thermal control system that shuts down if the CPU gets too hot; (2) Kikinis teaches a thermal control system that slows or stops the CPU clock if the CPU gets too hot; and (3) Gephardt teaches not to shut down a system if it is performing critical functions.

Representative claim 17 claims a computer with three means: (i) means for sampling temperature "associated with the operation of" a CPU, (ii) means for predicting temperature levels "associated with the operation of" a CPU, and (iii) means for using the prediction of temperature levels for automatic control of temperature. The Board found this claim to be obvious in view of (1) Hollowell (which teaches means for sampling temperature in a CPU for purposes of automatic temperature control), (2) Kikinis (which teaches means for sampling temperature and means for measuring temperature indirectly for purposes of automatic temperature control) and (3) Chen (which teaches sampling and predicting temperature in a CPU, and using the prediction for automatic temperature control).

The primary questions on appeal are whether substantial evidence supports the Board's findings as to claims 5 and 17.

STATEMENT OF THE CASE

In December 1995, LaVaughn F. Watts, Jr. ("Watts") filed the subject patent application, 08/568,904 (the "'904 application"),[2] entitled "Real-Time Thermal

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[2] Co-pending Appeal 03-1122 involves same inventor Watts' application 08/572,202 ("the '202 application"). Like the present '904 application, the '202 application is directed to a CPU thermal management system and was also filed in December 1995. In addition, the '202 application has virtually the same specification as the present '904 application, both stemming

Management for Computers." A15-16.[3] The patent examiner rejected for obviousness the claims currently on appeal in view of on the basis of either a combination of Hollowell, Kikinis and Gephardt, or a combination of Hollowell, Kikinis, and Chen. Watts appealed the examiner's decision to the Board (A214), which affirmed the examiner's decision on these claims (A11).

STATEMENT OF FACTS

A. Claimed Invention

Watts' application contains claims directed to preventing a CPU from overheating. A328-33. In claim 5, the CPU clock frequency is reduced when the CPU's temperature exceeds a certain level, provided the CPU is not processing critical input/output ("I/O"). A328. Thus, temperature is controlled by controlling the clock speed, except when critical I/O is being processed.

Claim 5 is representative of claims 2, 3, 5, 6, 9, 30, 31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67, and 71-73, and reads as follows:

5. An apparatus, comprising:

a provision for user input;

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from a common earlier application. Accordingly, a significant part of this Statement resembles that for 03-1122.

[3] The Appendix is referred to as "A___" and Watts' Brief is referred to as "Br. at ___".

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a monitor for monitoring temperature within said apparatus; and

a clock manager adapted to receive a control signal from said monitor, said clock manager selectively stopping clock signals from being sent to said central processing unit (CPU) when [i] said monitored temperature rises to a level at and above a selected reference temperature level and [ii] said CPU is not processing critical I/O.

A328.

The computer of claim 17 features "automatic control of temperature" based on predicted "temperature levels associated with the operation of a [CPU]." A329. Unlike claim 5, claim 17 does not contain a limitation regarding critical I/O.

Claim 17 is representative of claims 17-21 and 23,[4] and reads as follows:

17. A computer, comprising:

means for sampling a temperature level associated with the operation of a central processing unit within said computer;

means for predicting temperature levels associated with the operation of a central processing unit within said computer; and

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[4] The Board grouped claims 21 and 23 with the group of claims for which claim 17 is representative. As explained in Part C.3 of the Argument section below, although claims 21 and 23 would have been more appropriately grouped with claim 5, Watts' failure to follow the USPTO's rules regarding the content of his appeal brief estops him from now objecting to the Board's grouping.

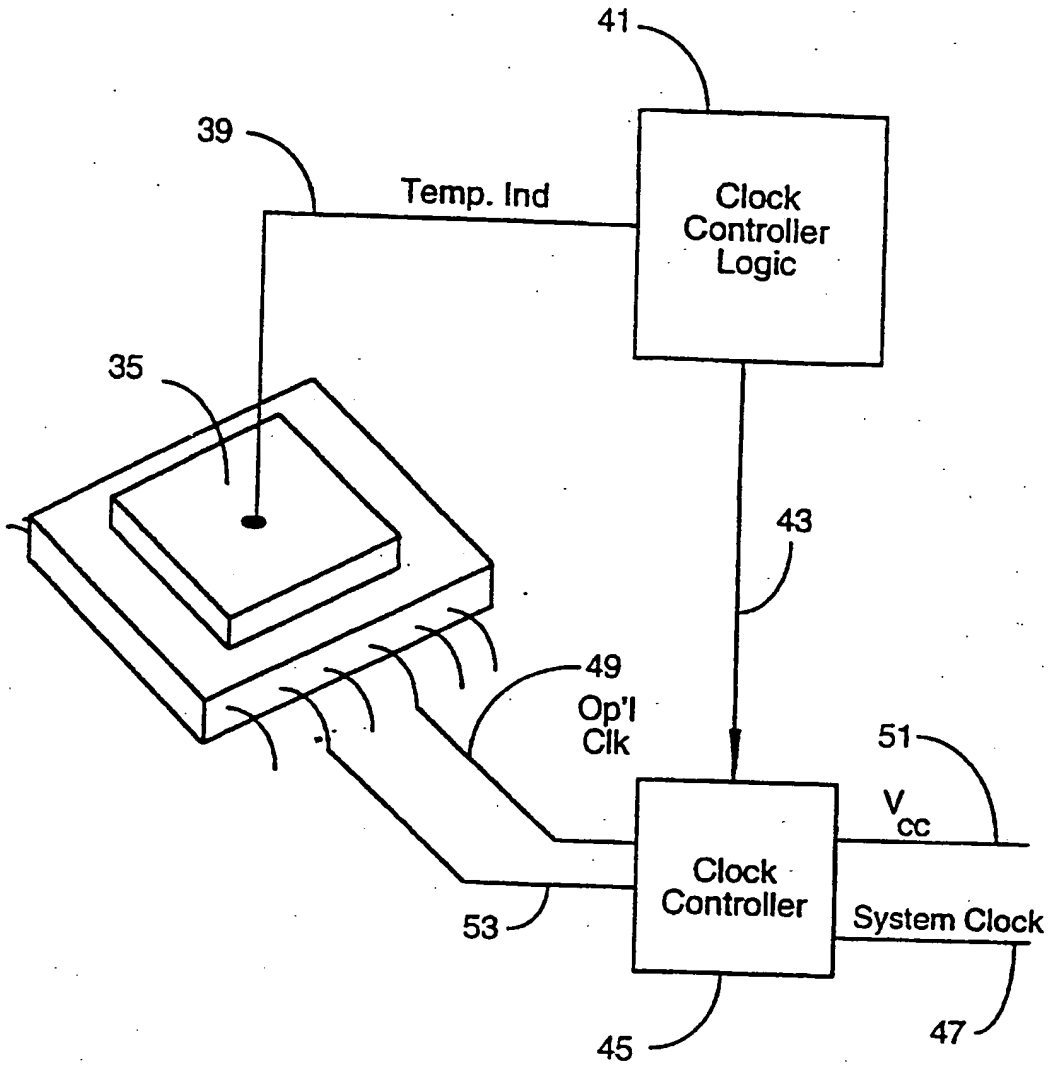
41
39
Temp. Ind
Clock Controller Logic
35
43
49
Op'l Clk
51
V_{cc}
Clock Controller
System Clock
53
45
47

FIG. 3

means for using said prediction for automatic control of temperature within said computer, said temperature control remaining transparent to a user of said computer.

A329.

B. Prior Art

The Board affirmed the examiner's obviousness rejection of claim 5 in view Hollowell, Kikinis, and Gephardt, all of which concern thermal management of CPUs. A11. The Board affirmed the examiner's obviousness rejection of claim 17 on the basis of the same first two references (Hollowell and Kikinis), but used a different third reference (Chen). Id.[5]

1. Hollowell: A CPU Thermal Management System

Hollowell discloses a thermal management system for a CPU that removes power to the CPU for short periods of time when a temperature sensor determines that internal system temperature has exceeded a certain level, A287, col. 3, lines 45-48; A279, Fig. 1; A287, col. 4, lines 47-48. Hollowell discloses a CPU coupled to user input and output. A279, Fig. 1 (opposite) (depicting coupling between processor 103, keyboard 122 and display 121); A287, col. 4, lines 42-45 ("alpha-numeric input device . . . for communicating information and command

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[5] See Hollowell U.S. Patent No. 5,590,061 (A278-93); Kikinis U.S. Patent No. 5,502,838 (A294-304); Gephardt U.S. Patent No. 5,493,684 (A305-319); Chen U.S. Patent No. 5,422,806 (A320-27).

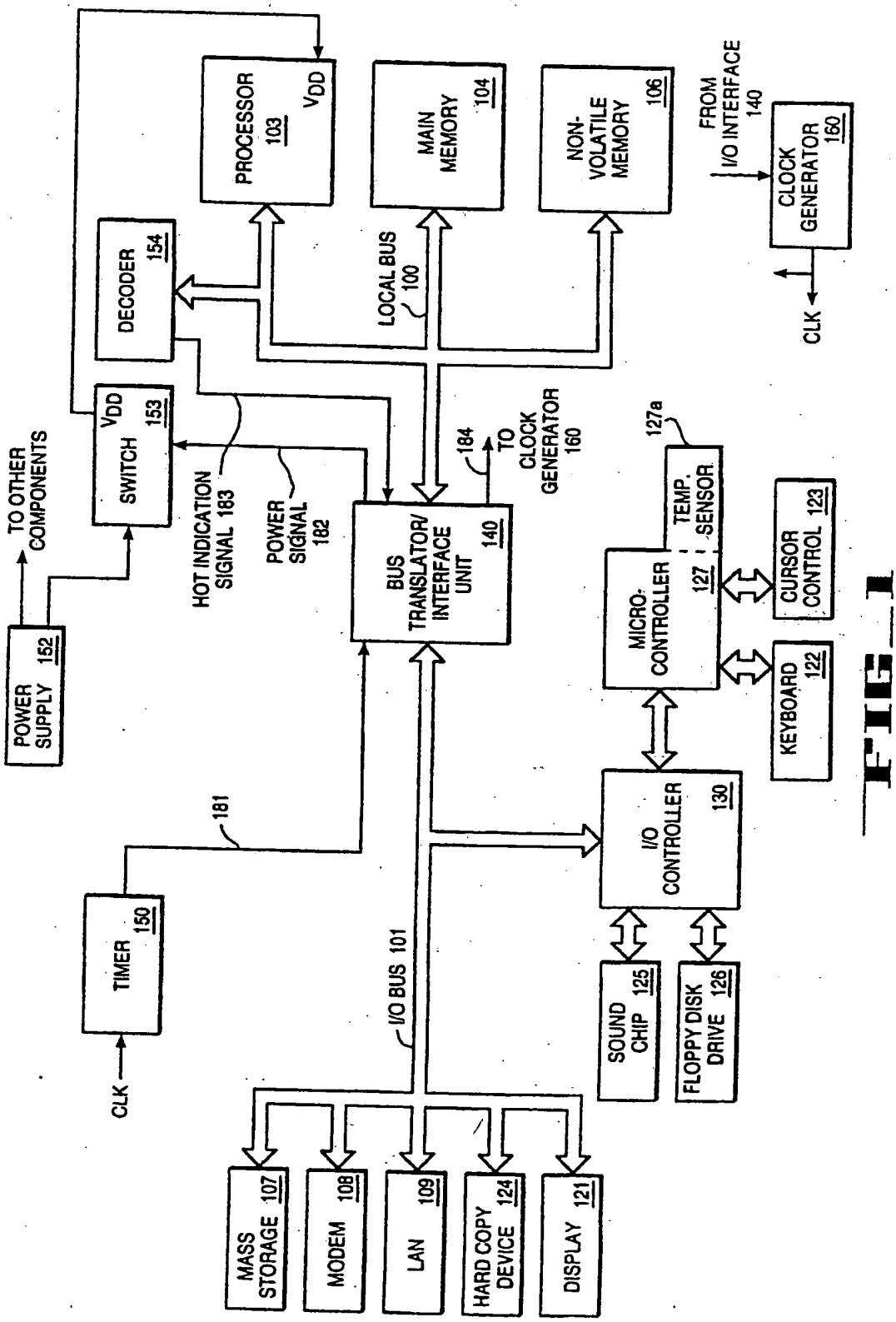
PROCESSOR 103 V_{DD}
MAIN MEMORY 104
NON-VOLATILE MEMORY 106
FROM I/O INTERFACE 140
CLOCK GENERATOR 160
CLK
DECODER 154
LOCAL BUS 100
V_{DD} SWITCH 153
TO OTHER COMPONENTS
HOT INDICATION SIGNAL 183
POWER SIGNAL 182
184
TO CLOCK GENERATOR 160
127a
TEMP. SENSOR
BUS TRANSLATOR/ INTERFACE UNIT 140
MICRO-CONTROLLER 127
CURSOR CONTROL 123
KEYBOARD 122
POWER SUPPLY 152
181
I/O CONTROLLER 130
TIMER 150
CLK
I/O BUS 101
SOUND CHIP 125
FLOPPY DISK DRIVE 126
MASS STORAGE 107
MODEM 108
LAN 109
HARD COPY DEVICE 124
DISPLAY 121

FIG. 1

selections to processor 103"); A287, col. 4, lines 21-24 ("A display device 121, such as a cathode ray tube . . . is also coupled to I/O bus 101 for displaying information to the computer user.").

2. Kikinis: CPU Thermal Management System That Stops Clock Signals

Kikinis discloses a thermal management system for a CPU that selectively stops clock signals to the CPU when temperature within the CPU exceeds a certain level. A294, Abstract; A297, Fig. 3; A300, Fig. 6.[6] As shown in Figure 3 (A297, opposite), Kikinis discloses clock controller circuit 45 (A302, col. 4, lines 30-32) which receives an input from "temperature sensor 35." A302, col. 4, lines 24-25. More specifically, "[a]n indication of temperature is delivered via line 39 to a logic control element 41" which then drives the clock controller and system clock. A301, col. 4, lines 26-30. Thus, in Kikinis the clock rate is driven by the temperature sensor. A301, col. 2, lines 19-24.

Kikinis also teaches "temperature-sensing circuitry" (A302, col. 3, lines 8-

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[6] Although Kikinis for the most part refers to "integrated circuits" and "microprocessors," it defines "microprocessor" as a preferred embodiment of an integrated circuit (A301, col. 2, line 25), and uses the term "CPU" interchangeably with "microprocessor." See A301, col. 1, lines 55-63 (noting that "[f]unctional units in a microprocessor are typically not used equally," and going on to note that "[a]s a result of this unequal utilization, some regions of a CPU generate heat, and therefore tend to increase in temperature, faster than other regions" (emphasis added)).

10), and explains that temperature may be measured indirectly, for example, based on the frequency of an oscillator circuit, or a rate of signal propagation. A302, col. 3, lines 19-41.

3. Gephardt: Does Not Slow or Stops Clock When Certain Types of Activity Are Occurring

Gephardt is concerned with power management within a CPU, which, as Gephardt recognizes, is related to solving the problem of excess heat generation in the CPU. A313, col. 1, lines 17-19 ("Reducing power consumption typically reduces heat generation of the system, thereby increasing reliability and descreasing cost."). Of particular pertinence here, Gephardt demonstrates that it was well-known in the art to distinguish between different kinds of activities in determining whether or not to stop a clock signal. Specifically, Gephardt describes prior art systems that "stop[] clock signals that drive inactive circuit portions" (A313, col. 1, lines 27-28), as well as systems that reduce the frequency of clock signals "that drive circuit portions during operating modes which are not time critical" (A313, col. 1, lines 35-36). In addition, Gephardt describes prior art power management units that, "[d]epending upon the detected activities, . . . may responsively power down selected circuit portions, reduce the frequencies of selected clock signals and/or completely stop selected clock signals." A313, col. 1, lines 47-50.

Gephardt itself concerns allocating power to different functions within a CPU, and teaches distinguishing between different types of computer operations in order to optimize power management. Thus, in Gephardt, "primary activities" are treated differently from "secondary activities." Whereas detection of a "primary activity" causes the system to change from any state to the "ready state" – the highest state of readiness – detection of a "secondary activity" causes the system to change to a "transitory state." Although both the "ready state" and the "transitory state," occur at maximum CPU clock frequency, the transition from the transitory state to a state in which clock signals are reduced or stopped occurs more quickly than for the ready state. A316, col. 7, line 60 - col. 8, line 55.[7] Moreover, while Gephardt's CPU clock signal cannot be slowed while the CPU is processing primary activity, it can be slowed when the CPU is processing

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[7] More specifically, after primary activities have ceased, the power management state machine transitions gradually from the ready state to the doze state, to the standby state, and finally to the suspend state. A316, col. 7, line 60 - col. 8, line 55. In contrast, when a power management state machine that was in the transitory state no longer detects secondary activities, it transitions directly to the state in which it was prior to entering the transitory state. A317, col. 9, lines 44-48. The impact on power management is that for the machine that was processing primary activities, the time to reach the suspend state – where the CPU clock signal will be stopped, and power to peripheral devices may be removed – is typically longer than for the machine that was processing secondary activities. See A314, col. 3, lines 4-16.

secondary activity.[8]

Gephardt's invention is not limited to a world in which activities are classified as either primary or secondary. In fact, claim 11 of Gephardt specifically claims three different types of internal activity, where the clock signal is controlled based on the type of internal activity. A318, col. 12, lines 54-63.

4. Chen: Thermal Management Based on Predicted Temperature

Chen, entitled "Temperature Control for a Variable Frequency CPU," also teaches controlling CPU temperature by controlling CPU clock signals. Rather than using actual temperature measurements as an input for the temperature control logic, however, Chen uses the variables time and operating frequency as a basis for predicting heat accumulation and heat dissipation – and thus temperature. A324, col. 1, lines 35-37. As the predicted temperature approaches a predetermined upper limit, CPU clock frequency is reduced. A324, col. 2, lines 21-24. Despite its focus on predicted temperatures, Chen also teaches using actual

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[8] Specifically, when a secondary activity is detected, Gephardt's state machine shifts from the current state (say, the standby state) to the "transitory state." The machine stays in the transitory state "for a predetermined time following detection of the secondary activity or for a predetermined amount of time following completion of the secondary activity." (A316, col. 8, lines 45-48). In cases where the machine stays in the transitory state "for a predetermined time following detection of the secondary activity," it is possible that the machine will transition back to the original state (and to a lower clock signal frequency) prior to completion of that activity.

temperature measurements for various purposes, including to calibrate the system. A324, col. 2, lines 48-50.

C. Board Decision

The Board considered the claims as two separate groups, represented by claims 5 and 17, respectively, consistent with Watts' statement of the issues and grouping of claims. A3 (stating that claims 2, 3, 5, 6, 9, 30, 31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67, and 71-73 stand rejected over Hollowell in view of Kikinis and Gephardt, and that claims 17-21 and 23 stand rejected over Hollowell in view of Kikinis and Chen); see also A217 (Watts' Appeal Brief) (setting forth these groupings as separate issues).

As to representative claim 5, the Board found that both Hollowell and Kikinis relate to "the control of heat generation within a computer in order to maintain the temperature within a desirable operating range." A7. Hollowell accomplishes this end by means of power control; Kikinis accomplishes the same result using frequency control. A7-8. Given the common subject matter, the Board found that one with skill in the art would have recognized that Hollowell and Kikinis teach different ways of accomplishing the same result, i.e., temperature control of a CPU. Therefore, the Board found that a computer designer would have been motivated to substitute the frequency control aspect of

Kikinis for the power control aspect of Hollowell. A7-8. The Board further found, based on Gephardt's teaching of not shutting down a computer while "primary" activities are occurring, that someone with skill in the art would have recognized the benefits of not slowing the clock signal for certain activities. A7-8.

As to claim 17, the Board found that the combination of Hollowell, Kikinis and Chen would have rendered the claim obvious. A10-11. The Hollowell-Kikinis combination taught temperature control of a CPU based upon measured temperatures; Chen teaches temperature control of a CPU based upon predicted temperatures. Based on Kikinis' suggestion that temperature could be measured indirectly, the Board found that it would have been obvious to modify the Hollowell-Kikinis combination to use indirect measurements of temperature – such as the predicted temperatures of Chen – to arrive at a device that controlled temperature based on predicted temperature information. A11.

SUMMARY OF ARGUMENT

Representative claim 5 is directed to an apparatus that "selectively stop[s]" clock signals from being sent to the CPU if (i) the CPU temperature rises above a reference level so long as (ii) the CPU is not processing critical I/O. Hollowell teaches a CPU thermal control system that shuts down the CPU if the CPU gets too hot and Kikinis teaches a thermal control system that slows or stops the CPU

clock if the CPU gets too hot. Kikinis teaches the benefits of using CPU clock control for CPU thermal management, thereby providing the motivation to combine Hollowell with Kikinis. A third reference, Gephardt, teaches not to shut down a CPU if it is performing critical functions. The benefit of not interrupting important system activities, as taught by Gephardt, is sufficient motivation to modify the Hollowell-Kikinis combination in view of Gephardt to arrive at the invention of claim 5. The Board's findings concerning the obviousness of claim 5 are therefore supported by substantial evidence.

Representative claim 17 claims a computer with three means: (i) means for sampling temperature "associated with the operation of" a CPU, (ii) means for predicting temperature levels "associated with the operation of" a CPU, and (iii) means for using the prediction of temperature levels for automatic control of temperature. The Hollowell-Kikinis combination discussed above in connection with claim 5 discloses means for sampling temperature and for providing automatic control of CPU temperature based on the sampled temperature. A third reference, Chen, teaches using a predicted temperature for automatic control of CPU temperature. Chen also discloses the benefits of using predicted temperature for temperature control, thereby providing motivation to include Chen's use of predicted temperature in the Hollowell-Kikinis combination. The Board's

findings underlying its obviousness conclusion as to claim 17 are therefore supported by substantial evidence.

ARGUMENT

A. Standard of Review

Watts must show that the Board erred in its obviousness conclusion, which this Court reviews de novo, or committed reversible error with respect to an underlying factual finding. In re Gartside, 203 F.3d 1305, 1315-16, 53 USPQ2d 1769, 1775-76 (Fed. Cir. 2000). What a prior art reference discloses is a question of fact. Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1088, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995). Similarly, whether a person of ordinary skill would have been motivated to combine prior art disclosures is also a question of fact. Gartside, 203 F.3d at 1316, 53 USPQ2d at 1776.

This Court upholds Board factual findings supported by substantial evidence. 5 U.S.C. § 706(2)(E); Gartside, 203 F.3d at 1315, 53 USPQ2d at 1775. Substantial evidence "is something less than the weight of the evidence but more than a mere scintilla of evidence," In re Kotzab, 217 F.3d 1365, 1369, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citation omitted), and "means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion," Consolidated Edison Co. v. NLRB, 305 U.S. 197, 229 (1938). "[T]he possibility

of drawing two inconsistent conclusions from the evidence does not prevent an administrative agency's finding from being supported by substantial evidence." Consolo v. Federal Maritime Comm'n, 383 U.S. 607, 620 (1966). Finally, whether an appellant preserved an argument below is a legal question "based on subsidiary factual findings." Cooper v. Goldfarb, 154 F.3d 1321, 1331, 47 USPQ2d 1896, 1904 (Fed. Cir. 1998); see also In re McDaniel, 293 F.3d 1379, 1382, 63 U.S.P.Q.2d at 1464 (Fed. Cir. 2002) (Board's "interpretation of [Rule 192] is normally entitled to considerable deference . . . [which] ordinarily will be accepted unless it is plainly erroneous or inconsistent with the regulation.").

B. The Board Properly Held That Claim 5 Would Have Been Obvious in View of Hollowell, Kikinis, and Gephardt.

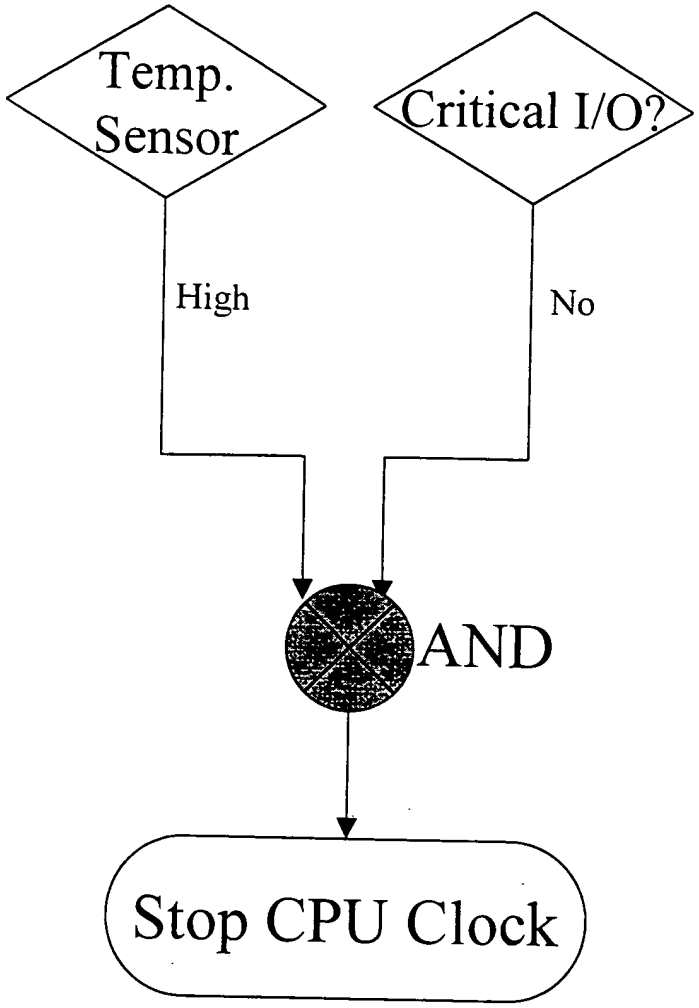
1. Representative Claim 5

Representative Claim 5 claims a CPU thermal management system that "selectively stops" clock signals when

(i) The CPU's temperature exceeds a reference level, and

(ii) The CPU is not processing "critical" I/O.

A328. Thus, claim 5's clock manager kicks in whenever the CPU (i) gets too hot and (ii) is not processing critical I/O. The next page shows a diagram of how the invention of claim 5 works.


Temp.
Sensor
Critical I/O?
High
No
AND
Stop CPU Clock

2. Every Element in Representative Claim 5 Is in the Prior Art.

Each and every element of claim 5 is found in the prior art, a fact that Watts did not dispute before the Board and does not dispute in his opening brief. Specifically, Hollowell discloses a CPU thermal management system having a user input and an output coupled to a CPU. A279, Fig. 1. It also discloses reducing CPU activity in response to increasing temperature. A278, Abstract.

The invention of claim 5 differs from Hollowell in that (1) it uses clock control rather than power control to reduce CPU activity, and (2) it specifies that CPU activity is not reduced when critical I/O is being processed. Kikinis and Gephardt supply the missing teachings. First, Kikinis teaches reducing CPU activity by controlling the CPU clock signal (A294, Abstract). Second, Gephardt teaches distinguishing between different types of CPU activity in terms of importance, and that clock frequency may be reduced for some activities but not others. A313, col. 1, lines 47-50.

The following claims chart compares representative claim 5 with the teachings of Hollowell, Kikinis, and Gephardt:

Representative Claim 5	The Prior Art Teaching
An apparatus, comprising:	Hollowell, passim; Kikinis, passim.

Representative Claim 5	The Prior Art Teaching
a provision for user input;	Hollowell, A279, Fig. 1; A287, col. 4, lines 42-45 ("alpha-numeric input device . . . for communicating information and command selections to processor 103")
a provision for output;	Hollowell, A279, Fig. 1; A287, col. 4, lines 21-24 ("A display device 121, such as a cathode ray tube . . . is also coupled to I/O bus 101 for displaying information to the computer user.")
a central processing unit (CPU) coupled to said user input and output;	Hollowell, A279, Fig. 1 (depicting coupling between processor 103, keyboard 122 and display 121).
a monitor for monitoring temperature within said apparatus; and	Hollowell, A279, Fig. 1; A287, col. 4, lines 47-48 ("temperature sensor 127A for measuring the internal system temperature") Kikinis, A302, col. 3, lines 8-10 ("[T]emperature-sensing circuitry is provided in the separate regions on the microprocessor IC where different functional units reside.")
a clock manager adapted to receive a control signal from said monitor,	Kikinis, A294, Abstract ("A system for controlling temperature buildup in an IC employs a temperature sensor to provide an indication of the IC temperature to a control circuit"); A297, Fig. 3; A300, Fig. 6.

Representative Claim 5	The Prior Art Teaching
said clock manager selectively stopping clock signals from being sent to said central processing unit (CPU) when said monitored temperature rises to a level at and above a selected reference temperature level	Kikinis, A294, Abstract ("a control circuit which is configured to provide an operational clock rate to the IC which is less than the system clock rate, based on a function of the temperature of the IC or its package.")
and said CPU is not processing critical I/O.	Gephardt, A305, Abstract (describing how the power management message unit encodes messages "[b]ased on detected activities," and how the power management unit "receives the encoded messages . . . and responsively makes decisions as to the appropriate power management mode to enter."); A311, Fig. 6 (depicting different power management modes for primary and secondary activities); A313, col. 2, lines 23-28 ("[A] variety of systems have been proposed in which the power management unit causes the frequencies of selected clock signals to be raised if certain system activities are detected and to be lowered if the system activities are not detected"); A314, col. 3, lines 22-24 ("Primary activities cause the power management unit to enter the ready state, regardless of the current state."); A317, col. 9, lines 27-33 (identifying various primary and secondary activities).

3. A Computer Designer Would Have Been Motivated To Combine Hollowell, Kikinis, and Gephardt To Arrive at the Invention of Claim 5.

To sustain an obviousness rejection established by combining the teachings of the prior art, there must be some suggestion, teaching, or motivation supporting the combination. In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998). The suggestion or motivation to combine references may flow from three sources: (1) the prior art; (2) the knowledge of one of skill in the art; or (3) the nature of the problem to be solved. Sibia Neurosciences Inc. v. Cadus Pharmaceutical Corp., 225 F.3d 1349, 1356, 55 USPQ2d 1927, 1931 (Fed. Cir. 2000).

Here, Hollowell is relied on for little more than the CPU itself. Kikinis and Gephardt both teach useful features for preventing excessive heat generation in a CPU, and thus Kikinis and Gephardt both contain motivation to combine them with Hollowell. More specifically, Hollowell teaches a CPU having an input and an output, Kikinis teaches a thermal management system for a CPU, and Gephardt teaches that an otherwise-appropriate reduction of CPU activity levels should not be initiated while certain activities are occurring. The examiner easily established a prima facie case for the combination based on the fact that the two references that were combined with Hollowell taught that they would be useful enhancements

to a CPU.

a. The Hollowell-Kikinis Combination: The Use of Hollowell's Input and Output Provisions With Kikinis' Clock Control Was Obvious.

Hollowell teaches including a provision for user input and a provision for output on a CPU (A279, Fig. 1), and also teaches a teaches a thermal management system that controls CPU temperature by controlling power to the CPU (A287, col. 3, lines 45-48). Like Hollowell, Kikinis also teaches a thermal management management system for a CPU, but like claim 5, Kikinis controls temperature by controlling the CPU clock frequency. A294, Abstract. Thus, it would been obvious to replace Hollowell's power control with Kikinis's clock control to arrive at a CPU having user input and output as well as Kikinis' thermal management system. The motivation for doing so is provided by Kikinis, which teaches the advantages of using clock control for CPU thermal management. See, e.g., Kikinis, A303, col. 5, lines 29-32 (explaining that "voltage may be lowered for a lower clock rate, thereby saving power use and further temperature increase").

Watts' criticism that "the Board does not explain how one having ordinary skill in the art would cut out the power control techniques in Hollowell and substitute therefore [sic] Kikinis' frequency control without undue experimentation" (Br. At 36) misses the point. Kikinis itself teaches that its

frequency control can be used with a CPU. No additional teaching is necessary to support the substitution for purposes of the obviousness inquiry. See, e.g., In re Sneed, 710 F.2d 1544, 1550, 218 U.S.P.Q. 385, 389 (Fed. Cir. 1983) ("[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review.").[9]

b. It Was Known To Not Stop Clock Signals to the CPU When Important Activity Was Occurring.

The only limitation of claim 5 not found in the Hollowell-Kikinis combination is the provision that clock signals are not stopped when the CPU is processing "critical I/O." A328. Watts did not offer a definition of "critical I/O" in either his specification or his brief. The most context that the specification gives to the term "critical I/O" is the following paragraph:

> The power conserving thermal management system asks the CPU questions such as are you doing something now that I cannot go do? If not, please sleep. If yes, don't sleep and come back to me so that I can reset my count. The result is a graduated effect up and graduated effect down and the thermal read constant time period adjusts itself in response to CPU temperature. Performance taken away from the user during power conservation and thermal management control is

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[9] Another way of viewing the Hollowell-Kikinis combination would be to consider whether there was motivation to add Hollowell's input and output to Kikinis' CPU. Because the benefits to a CPU of input (a keyboard) and output (a monitor) are readily apparent (for example, to enable a user to interact with the CPU), if not inherent, adding these features from Hollowell to Kikinis' CPU was obvious.

balanced against critical I/O going on in the system.

A36.

Thus, the specification unhelpfully indicates that "critical I/O" is (with the CPU as "you" and the thermal management system as "I") : "something [that you are doing] now that I cannot go do [sic]." The only example of "critical I/O" provided in the specification is that of a "wave file being played." A36. The only dictionary definition of "critical" that is even arguably close to what appears to be Watts' meaning is "Indispensable, vital" (Webster's Ninth New Collegiate Dictionary at 307(Merriam Webster 1990)), but it is difficult to see how playing a wave file could be considered "indispensable" or "essential."

In view of the Board's obligation to construe claims as broadly as is reasonable and consistent with the specification, see, e.g., In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000), an appropriate definition of the term "critical I/O", consistent with the specification's usage, is activities during which it would be undesirable to stop or slow the CPU clock. Gephardt provides the missing teaching by providing examples – from both the prior art and Gephardt itself – where clock signals are controlled based on the type of activities occurring.

Like Hollowell and Kikinis, Gephardt involves controlling a CPU to

prevent, among other things, overheating. Specifically, Gephardt describes a power management system that controls the frequency of the CPU clock in order to reduce power consumption. As Gephardt explains, "[r]educing power consumption typically reduces heat generation of the system, thereby increasing reliability and decreasing cost." A313, col 1, lines 17-19.

Gephardt teaches that it was known to control the CPU clock signal based on the type of activity that was occurring. See A313, col. 1, lines 47-50 (describing prior art power management units that, "[d]epending upon the detected activities, . . . may responsively power down selected circuit portions, reduce the frequencies of selected clock signals and/or completely stop selected clock signals."); A313, col. 1, lines 27-28 (describing prior art systems that "stop[] clock signals that drive inactive circuit portions"); id. at col. 1, lines 35-36 (describing prior art systems that reduce the frequency of clock signals "that drive circuit portions during operating modes which are not time critical").

Gephardt itself provides an example of a system that slows and stops clock signals to conserve power (and thus prevent excessive heat generation) except when certain activities are occurring. See A314, col. 3, lines 10-13 (explaining that during "doze" state, frequency of CPU clock is slowed, and that during "stand-by" state, frequency of CPU clock is stopped); A314, col. 3, lines 5-8

(explaining that CPU clock signal is driven at maximum frequency if primary activity is detected); A314, col. 3, lines 22-24 (explaining that primary activities cause the computer to enter the ready state regardless of its current state); A314, col. 3, lines 15-21 (explaining that CPU clock signal is increased to maximum frequency if secondary activity is detected).[10]

Accordingly, Gephardt teaches claim 5's limitation of not stopping clock signals when "critical I/O" is being processed. There was strong motivation to add this feature to the Hollowell-Kikinis combination, in order to prevent the interruption of important activities and potential loss of information that could be caused by reducing the clock signal or shutting down the computer while such activities were occurring. As Gephardt explains, by distinguishing between types of activity in this manner, "flexibility and optimization of power management may be attained." A314, col. 3, lines 33-34.

(i) The Fact That Gephardt's "Secondary" Activities May Be Processed at Full Clock Speed Supports the Board's Decision.

Watts makes much of what he believes is an error in the Board's discussion of primary and secondary activities. According to Watts, the Board's discussion

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[10] As discussed below in section B.3.b(i), the fact that both primary and secondary activities are typically processed at full clock speed does not help Watts' argument.

of primary and secondary activities implies that the Board believed that secondary activities are not processed at full clock speed. See Br. at 41. Despite Watts' characterization of the Board's opinion, the Board never stated that it believed that Gephardt's secondary activities were processed at anything other than full clock speed, nor did it state that secondary activities could not be considered "critical." Rather, the Board merely noted that the distinction between primary and secondary activities suggested that "some activities are considered to be more critical than other activities." A8.

The fact that Gephardt's secondary activities are typically processed at full clock speed (see A314, col. 3, lines 15-21) is itself a basis for rejecting Watts' strained interpretation of the Board's decision to the contrary. Gephardt's teaching that the CPU should continue to operate at full clock speed while certain important activities are occurring (regardless whether those activities are classified as primary or secondary) is more than sufficient to suggest to someone with skill in the art that clock signals should not be stopped when the CPU is processing so-called "critical" I/O.[11]

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[11] Moreover, Watts is simply incorrect in his assertion that secondary activities are always processed at full clock speed. See supra n. 8.

C. Claim 17 Is Obvious in View of Kikinis, Hollowell, and Chen.

Claim 17 claims a computer with three means:

(i) a means for sampling the temperature level of the CPU;

(ii) a means for predicting temperature levels of the CPU; and

(iii) a means for using the predicted temperature for automatic control of temperature within the computer.

A329. The support for claim 17 is presumably found in the following paragraph of the specification:

> "Thermal management can be also be [sic] achieved using a prediction mode. Prediction mode utilizes no sensors or thermistors or even knowledge as to actual CPU temperature. Prediction mode uses a guess – i.e. that the system will need the ad hoc interrupt once every 5 seconds or 50 times/second (=constant) and then can take it up or down based on what the system is doing with the active power and thermal management. The prediction theory can also be combined with actual CPU temperature monitoring."

A37.

Thus, although it is not entirely clear, it appears that claim 17 measures actual temperature, predicts temperature, and uses the predicted temperature to control the temperature of the CPU. The predicted temperature (or "prediction mode") is <u>not</u> the actual temperature of the CPU. Rather, it is a guess at what the temperature of the CPU is, based on, for example, something the CPU is doing

(e.g., clock speed, time, etc.).

1. All the Limitations of Claim 17 Are Taught by Hollowell, Kikinis and Chen.

As already discussed, there was motivation to combine Hollowell with Kikinis to arrive at a device that controls temperature by controlling CPU clock speed in response to actual temperature measurements. Chen teaches using predicted temperature measurements instead of actual temperature measurements for clock control in a thermal management system. A327, col. 7, lines 4-24. Thus, the combination of Hollowell, Kikinis and Chen contains all of the limitations of claim 17. The following table compares claim 17 to these three references.

Claim 17	Hollowell	Kikinis	Chen
17. A computer, comprising:	passim	passim	passim

Claim 17	Hollowell	Kikinis	Chen
means for sampling a temperature level associated with the operation of a central processing unit within said computer;	A279, Fig. 1; A287, col. 4, lines 47-48 ("temperature sensor 127A for measuring the internal system temperature")	A302, col. 3, lines 8-10 ("[T]emperature-sensing circuitry is provided in the separate regions on the microprocessor IC where different functional units reside.")	A320 (Abstract) (""The estimate is modeled after actual temperature change measurements" (emphasis added)); A324, col. 2, lines 45-50 ("[A] piecewise estimate of temperature change is employed, which . . . may be adjusted or calibrated in accord with realistic measurements or estimates of actual temperature conditions).
means for predicting temperature levels associated with the operation of a central processing unit within said computer; and	–	A302, col. 3, lines 19-41 (noting that an indication of temperature may be obtained, for example, based on the rate of signal propagation from a functional area.)	A327, col. 7, lines 4-24 (claim 1) (describing correlating measurements of elapsed time and frequency with piecewise estimate of CPU temperature change to obtain estimated temperature)

Claim 17	Hollowell	Kikinis	Chen
means for using said prediction for automatic control of temperature within said computer, said temperature control remaining transparent to a user of said computer.		A294, Abstract ("a control circuit which is configured to provide an operational clock rate to the IC which is less than the system clock rate, based on a function of the temperature of the IC or its package.")	A327, col. 7, lines 22-24 (claim 1) ("throttling the CPU frequency if the piecewise estimate of CPU temperature approaches said upper limit".

Although it appears from the table above that either Kikinis or Chen alone teaches all the limitations of claim 17, the examiner chose to rely on the combination of Hollowell and Kikinis, plus Chen, as the basis for an obviousness rejection. The Board properly upheld the examiner's rejection.

2. There Was Ample Motivation To Combine Chen With Hollowell and Kikinis.

The Hollowell-Kikinis combination is a thermal management system that samples temperature and that controls temperature by slowing or stopping the CPU clock. Moreover, Kikinis itself teaches that the temperature upon which frequency control is based can be derived from an indirect measurement, including the rate of signal propagation. A302, col. 3, lines 19-41.

Chen provides more specific teachings on the manner in which temperature might be predicted, including predicting it based on time and operating frequency. A324, col. 1, lines 35-37. Specifically, Chen teaches the benefits of predicting temperature (see, e.g., A324, col. 1, lines 30-33 (explaining the cost savings associated with a thermal management system that uses predicted temperature rather than actual temperature)); and thus itself provides the motivation to combine Chen with the Kikinis-Hollowell combination to arrive at the computer system of claim 17.

Watts points out that the Board, in affirming the examiner's rejection, indicated that the rejection was based on "'replac[ing] the actual temperature measurements of Hollowell or Kikinis with predicted temperature measurements as taught by Chen.'" Br. at 51 (quoting Board Decision at A10). However, if one looks to the examiner's reasoning, which the Board affirmed, one finds:

> "As per claims 17, 18 and 21, Hollowell and Kikinis disclose the claimed invention including monitoring temperature levels in a computer. However, Hollowell and Kikinis do not teach predicting activity and temperature levels relevant to the operation of a CPU within the computer and using the predictions for automatic temperature control. Chen teaches that it is known to predict activity levels within a computer and using the prediction for automatic control and also, remain transparent to the user (col. 7, lines 4-24). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Chen, since having the capability to predict temperature rises and automatically control them, prior to the occurrence could prevent

premature failure of the CPU or circuit components."

A251-A252 (emphasis added).

Thus, the combination that was upheld by the Board did not "replace" the temperature measurement of Hollowell and Kikinis, but rather included Chen's use of predictions for automatic control in the Hollowell-Kikinis combination. See 37 C.F.R. § 1.196(a) ("The affirmance of the rejection of a claim on any of the grounds specified constitutes a general affirmance of the decision of the examiner on that claim, except as to any ground specifically reversed."). As such, the combination of Hollowell, Kikinis and Chen meets all the limitations of the claimed invention. Moreover, given that all three of Hollowell, Kikinis, and Chen teach circumstances under which actual temperature measurements are made, and given that the "temperature sampling" limitation from claim 17 is unconnected to any other element in the claim, the inclusion of "temperature sampling" does not patentably distinguish claim 17 from the prior art.

3. Claim 21 Did Not Require Separate Consideration by the Board.

The Board treated claim 17 as representative of claims 21 and 23 (which is dependent on claim 21), and therefore rejected those claims on the same basis (Hollowell, Kikinis, and Chen). On appeal, Watts argues that since claim 21 contains a "critical I/O" limitation that is not taught by any of the three cited

references, the Board's rejection was improper. Watts' argument is untimely and irrelevant, in view of Watts' appeal brief's failure to comply with rule 37 CFR 1.192's provisions regarding separately argued claims, as well as Watts' own grouping of claim 21 with claim 17 in that brief.[12]

a. Watts Failed To Sufficiently Argue Claim 21 to the Board.

Pursuant to Rule 1.192, Watts was required to provide a clear statement for each rejection indicating whether the claims subject to that rejection stand or fall together, as well as non-conclusory arguments explaining why each separately-argued claim or group of claims was patentable. Rule 1.192(c)(7) provides:

> **Grouping of claims.** For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

37 C.F.R. 1.192(c)(7). This Court has recently explained:

> [Rule 1.192(c)(7)] operates to relieve the Board from having to

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[12] Claim 23 adds to claim 21 the limitation "wherein said adjustments are accomplished within the central processing unit (CPU) cycles and do not affect the user's perception of performance." A330. Because Watts has not argued in this appeal that this additional limitation imparts patentability to this claim, claim 23 should stand or fall with claim 21.

> review . . . the myriad of distinctions that might exist among claims, where those distinctions are, in and of themselves, of no patentable consequence to a contested rejection . . . . The rule acts as the default that permits the Board to designate one claim to serve as representative of others in a commonly rejected group and to focus its attention on only those matters that are dispositive of the appeal, *unless applicant overcomes the default to assure separate review of individual claims by meeting the two conditions specified in the rule.*

In re McDaniel, 293 F.3d at 1383, 63 U.S.P.Q.2d at 1464.

In this case, appellant's appeal brief did not satisfy either of the two conditions of Rule 1.192 as to claim 21. It (1) failed to provide a clear statement that claim 21 did not stand or fall with claim 17, and (2) failed to provide a sufficient explanation in its brief as to why it was separately patentable.

(i) Watts' Appeal Brief Failed To Provide a Sufficient Explanation as to why Claim 21 Was Separately Patentable.

In stark contrast to the requirements of Rule 1.192, Watts' appeal brief repeatedly made vague and conclusory arguments as to why various claims were patentable. For example, Watts' argument as to claim 2, in its entirety, reads:

> "Claim 2 further defines the apparatus of Claim 5 wherein said user input is coupled to a keyboard. The Hollowell, Kikinis, and Gephardt references fail, alone or combination, to teach or suggest this further limitation in combination with the requirements of Claim 5."

A225. See generally A225-A234 (providing similarly conclusory arguments as to why numerous other claims are patentable); see also Hollowell, A279, Fig. 1

(depicting a keyboard). The Board properly rejected this mode of argumentation. A9 (explaining that "neither of the two types of appellant's arguments . . . constitutes a persuasive argument that the rejection is in error.").

Watts' argument as to claim 21 was similarly vague and conclusory. After quoting from claim 21, Watts provided a one-paragraph argument:

> "As stated above, Chen teaches a temperature prediction mode in which NO TEMPERATURE MEASUREMENTS ARE NEEDED OR MADE (col. 2, lines 44-45). Kikinis, on the other hand, discloses a device in which temperature measurements ARE MADE – i.e., which selectively stops clock signals when the detected temperature rises above a reference temperature level. Kikinis fails, however, to teach or suggest that the selective stopping be performed only when the monitored temperature is at or above a selected reference and said CPU is not processing critical I/O. Kikinis also fails to teach or suggest any modification of the clock signal to the processor for any reasons other than temperature. Any combination of Chen, Kikinis and Hollowell, fails to address the discrepancies between, or justify any combination of the Chen and Kikinis (regarding temperature measurements and temperature prediction) with the Hollowell reference. Moreover, none of the references (alone or in combination) teach or suggest that critical I/O will, or should, affect the performance of the temperature reduction mechanism."

A233-234.

Especially in view of the numerous meritless and conclusory arguments that preceded this paragraph, Watts was obligated to provide a clear argument here as to why the asserted references failed to teach or suggest the "critical I/O" limitation. Instead, Watts repeated his pattern of making vague and conclusory

statements rather than arguments.[13] Under these circumstances, the Board was entitled to group this claim with claim 17, and dispose of it accordingly.

(ii) Watts' Own Claim Grouping Grouped Claim 21 With Claim 17.

Pursuant to Rule 1.192, Watts was required to provide a clear statement for each rejection indicating whether the claims subject to that rejection stand or fall together. If the appeal brief does not contain

> "a clear statement for each rejection . . . asserting that the patentability of claims within the group of claims subject to this rejection do not stand or fall together, . . . the Board is free to select a single claim from each group of claims subject to a common ground of rejection as representative of all claims in that group and to decide the appeal of that rejection based solely on the selected representative claim."

In re McDaniel, 293 F.3d at 1383, 63 U.S.P.Q.2d at 1465. Watts failed to provide separate statements for the two rejections on appeal, and the single statement that he did provide was far from clear.

The "Grouping of Claims" section of Watts' Brief to the Board consisted of the following statement:

> "Claims 2, 3, 5, 6, 9, 17-21, 23, 30, 31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67, and 71-73 stand or fall separately."

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[13] In In re Thrift, 298 F.3d 1357, 63 U.S.P.Q.2d 2002 (Fed. Cir. 2002) a case involving the same assignee and same attorney for appellant, the court similarly held that conclusory arguments were insufficient to preserve issues for appeal. Id. at 1360, 63 U.S.P.Q.2d at 2003.

A217. The most logical interpretation of this statement is that any individual claim or group of claims linked by a hyphen should be understood to stand or fall separately from each of the other claims or groups of claims. If the hyphen were intended merely to link successive claim numbers (and not to designate groups), then hyphens would have appeared between claims 2 and 3, 5 and 6, and 30 and 31. Under any other interpretation, Watts has used hyphens inconsistently.[14] Accordingly, Watts himself grouped claim 21 with claim 17. Based on this grouping, the Board was not required to consider claim 21 separately from claim 17.

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[14] Any argument that Watts was following a convention of hyphenating only when there were more than two successive claims is belied by Watts' issue statement – which appeared on the same page as Watts' claim grouping – and in which Watts hyphenates groups of two successive claims:

> "1) Are claims 2-3, 5-6, 9, 30-31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67, and 71-73 patentable under 35 U.S.C. § 103 over Hollowell, II et al. In [sic] view of Kikinis and further in view of Gephardt et al?
>
> "2) Are claims 17-21 and 23 patentable under 35 U.S.C. § 103(a) over Hollowell, II et al in view of Kikinis and further in view of Chen et al?"

A217. It is also worth noting that the issue statement was another missed opportunity for Watts to spell out his argument that claim 21 should be considered separately from claim 17. Like the grouping of claims, the issue statement fails to provide any hint that claim 17 might not be representative of claim 21.

Watts' treatment of claims 17-21 is further evidence that his statement that claims "17-21 . . . stand or fall together" should be interpreted as grouping claims 17-21 as a single group. Watts makes the same arguments as to claims 17 and 18 (A231-33), and makes no argument whatsoever as to claims 19 and 20. Watts' combined treatment of claims 17 and 18, plus his failure to make any argument as to claims 19 and 20, requires that Watts' claims grouping be interpreted to designate claims 17-21 as a single group.

Thus, because of his decision to bury his argument as to claim 21 in a morass of improper make-weight arguments, plus his failure to provide a clear statement as to claim groupings, Watts has only himself to blame for the fact that the Board did not consider the argument as to claim 21.[15]

b. Any Error By the Board Can Be Expeditiously Addressed on Remand.

As explained above, we do not believe that the Board erred in failing to consider more closely Watts' arguments as to claim 21. Nevertheless, in the event that the Court finds that Watts' arguments and claim grouping were sufficiently specific to meet the requirements of Rule 1.192 and In re McDaniel, the Court

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[15] Rule 1.192 is designed to allow the Board to do exactly what the Board did here: cut through the case to what appears to be genuinely disputed. In this case, the dispute about claim 21 was so well concealed by Watts's non-compliance with Rule 1.192 that the Board did not – and was not required to – take note of it.

should remand to the Board for consideration of those arguments. However, we note that the Board's determination of unpatentability as to claim 5 will dictate its conclusion as to claim 21.

The following chart compares claim 5 with claim 21:

Claim 5	Claim 21
An apparatus, comprising:	An apparatus, comprising:
a provision for user input;	
a provision for output;	
a central processing unit (CPU) coupled to said user input and output;	a central processing unit (CPU);
a monitor for monitoring temperature within said apparatus; and	means for sampling a temperature level within said apparatus;
a clock manager adapted to receive a control signal from said monitor,	
said clock manager selectively stopping clock signals from being sent to said central processing unit (CPU) when said monitored temperature rises to a level at and above a selected reference temperature level	means for automatically adjusting the processing speed of said central processing unit (CPU) by modifying the clock signal utilized by the central processing unit (CPU) to maintain said temperature level within said apparatus below a selected reference temperature level
and said CPU is not processing critical I/O.	when said CPU is not processing critical I/O.

As can be seen from this table, several limitations that are present in claim 5 are not present in claim 21. Where corresponding limitations appear, claim 21 is

in every respect as broad or broader than claim 5. For example, the "clock manager selectively stopping clock signals" of claim 5 corresponds to and is narrower than the "means for automatically adjusting the processing speed of said central processing unit (CPU) by modifying the clock signal" of claim 21: a clock manager is just one "means for automatically adjusting the processing speed." Similarly, "selectively stopping clock signals" is just one way of "modifying the clock signal." In addition, the aspirational aspect of this limitation of claim 21 – "to maintain said temperature level within said apparatus below a selected reference temperature level," is essentially equivalent (and certainly not patentably distinguishable) from claim 5's requirement that the clock signals be selectively stopped when temperature exceeds a reference level.

Indeed, Watts' arguments for the patentability of claim 21 are identical to those he makes for claim 5. Compare Br. at 25-26 (arguing that claim 21 is patentable over Hollowell, Kikinis and Gephardt because Gephardt, according to Watts, "fails to teach 'reducing or slowing a clock signal to a CPU ONLY when the CPU is not processing critical I/O") with Br. at 23-24 (making the same argument for claim 5). Accordingly, given that claim 21 was broader than claim 5, the fact that claim 5 was obvious over the combination of Hollowell, Kikinis, and Gephardt necessarily means that claim 21 was obvious over those same references.

CONCLUSION

Since Watts has failed to show that the Board committed any reversible error in its decision, this Court should affirm the Board's decision.

Respectfully submitted,

JOHN M. WHEALAN
Solicitor

THOMAS W. KRAUSE
JOSEPH G. PICCOLO
Associate Solicitors

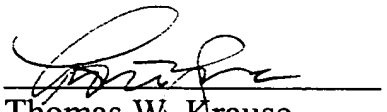
P.O. Box 15667
Arlington, Virginia 22215
(703) 305-9035

Attorneys for the Director of the United States Patent and Trademark Office

May 21, 2003

RULE 32(a)(7)(c) CERTIFICATE OF COMPLIANCE

I, Thomas W. Krause, Associate Solicitor and an attorney of record for the Appellee Director of the United States Patent and Trademark Office do hereby certify pursuant to FRAP 32(a)(7) that the foregoing brief complies with the type-volume limitation. The total number of words in the foregoing brief, excluding the table of contents and table of authorities, is 8702, as calculated by the WordPerfect 9.0 program.



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Associate Solicitor

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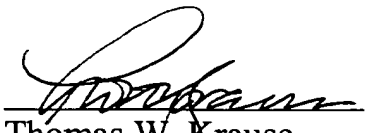

Thomas W. Krause
Associate Solicitor